REMARKS

Status of Claims:

Claim 2 has been cancelled. New claim 11 has been added. Thus, claims 1, and 3-11 are present for examination.

Prior Art Rejection:

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as unpatentable over applicant's admitted prior art (APA) in view of Van Roozendaal (5,281,841) or Duvvury (5,502,317).

The Examiner recognizes that APA does not teach a first conductive type well formed directly under the first source diffusion layer with the first conductive type well electrically connected directly with the source diffusion layer and at least partially underlying the element isolation film. Moreover, APA does not disclose that the first conductive type well has a lower dopant concentration than the source diffusion layer.

The Examiner has cited has cited Van Roozendaal and/or Duvvury to supply the missing ingredients. In order to better differentiate applicant's invention from the applied prior art, applicant has amended the independent claims to recite a channel region between the source and drain diffusion layers and to further recite that the source and drain diffusion layers each have extension regions formed in said channel region and not extending between the source and drain diffusion layers and the first conductive type well. Moreover, applicant's independent claims further recite that the extension regions have a dopant concentration between the dopant concentration of the source and drain diffusion layers and the first conductive type well. Applicant's extension regions are illustrated, for example, at element 12 in Fig. 2. As may be seen from Fig. 2 (as well as Fig. 3), the extension regions extend in the channel region which is formed between the source and drain diffusion layers but does not extend in the area between the in-type well and the source. Further, the concentration of the extension region is between the concentration of the well and the source/drain diffusion layers. See, for example, applicant's specification on page 19, lines 14-16, and on page 20, line 7.

In contrast, Van Roozendaal discloses the source and drain regions, each having a highly doped subsidiary region 220b (for the source) and a relatively lowly doped subsidiary region 22a (for the source). The relatively lowly doped subsidiary region 22a extends within the channel but also extends underneath the highly doped subsidiary region 22b and thus underneath the electrode 28 and, most importantly, is interposed between the relatively lowly doped well 22d and the highly doped subsidiary region 220b. The structure is specifically excluded by applicant's claim recitation wherein the extension regions do not between the source and drain diffusion layers and the first conductive type well. Moreover, Van Roozendaal appears to disclose that the subsidiary region 22a and the well 22d both have the same concentration since they both are characterized as "relatively lowly doped" regions. Thus, Van Roozendaal does not disclose the additional claim limitations now recited in applicant's independent claim, namely, that the extension regions have a dopant concentration between the dopant concentration of the source and drain diffusion layers and the first conductive type well.

The Duvvury patent cited by the Examiner does not disclose the structured note concentrations of the extension regions as recited in the applicant's claims.

With respect to newly added claim 11, applicant points out that claim 11 is an independent version of un-amended dependent claim 2 (now cancelled). This claim is likewise deemed patentable especially in view of the further explanation of the references as set forth below.

In particular, in Van Roozendaal the relatively deep relatively lowly doped n conductivity type well regions 21d and 22d are not essential but assist in avoiding spiking that is shorting of the source or drain region to the semiconductor body or substrate 10 caused by diffusion of the metallization material through the source or drain region into the substrate or semiconductor body 10. (See column 8 line 54-65)

For the purpose of avoiding "spiking" due to metal diffusion, the depth of n wells to be formed under the source and drain region should be chosen based on the diffusion length of metal used for the source and drain electrodes (21c and 22c). If the diffusion length of

metal is substantially smaller than the depth of the p well (semiconductor body 10), there is no reason to select the depth that the bottom of n well (21d and 22d) is being the same depth as the bottom of the p well (10) or at a level deeper than the bottom of the p well (10) as recited in the claims. In order words, Van Roozendaal does not provide any clear teaching about such selection that "the bottom of said first conductive type well (n well 1a) is formed at the same depth as the bottom of the second conductive type well (p well) or at a level deeper than the bottom of the second conductive type well (p well 2)", which is one of characteristic features of Claim 11.

In addition, such choice that the depth of n well 1a is the same or larger than the depth of p well 2 will provide the following advantage. In particular, with such a structure, after breakdown of the drain section, current flows through the semiconductor substrate 20 that has a higher resistance than the p well 2, which facilitated the potential of the base region of the parasitic bipolar transistor to rise and, therefore, makes the trigger voltage Vt1 lowered more efficiently. (See Fig. 4 and Fig. 5 of the present application)

In greater detail, Van Roozendaal teaches a device structure as shown in Fig. 6 where n well 21d is formed under drain region 21, and n well 22d is formed under source region 22. However, Van Roozendaal does not teach a device structure wherein the n well 22d is formed under source region 22 but n well 21d is not formed under drain region 21.

The internal circuit of the N-MOS FET, shown in Fig. 6, is illustrated by the circuit diagram of Fig. 7.

The protection element 20 thereof is sued in such a condition that the source 22 and p-well 10 (semiconductor body or substrate) are electrically connected to Vss (ground) level and the drain 21 is electrically connected to bias V (input/output). In such case, the shorting of source region to the p-well 10 (semiconductor body or substrate) has no effect on the performance of the protection element 20, but the shorting of drain region to the p-well 10 (semiconductor body or substrate) has a significant effect. Therefore, only the n well 21d formed under drain region 21 is essential, but the n well 22d formed under source region 22 is by no means essential.

Accordingly, in the case where the source 22 and p-well 10 (semiconductor body or substrate) are electrically connected to the Vss (ground) level and the drain 21 is electrically connected to the bias V, Van Roozendaal does not disclose the protection circuit structure such that the n well 22d is formed under source region 22 but the n well 21d is not formed under drain region 21.

In other word, Van Roozendaal does not provide any suggestion that such a structure in which the n well 22d is formed under source region 22 but the n well 21d is not formed under drain region 21 may be meaningful for the case where the source 22 and p-well 10 (semiconductor body or substrate) are electrically connected to the Vss (ground) level and the drain 21 is electrically connected to bias V.

As for Duvvury, one embodiment for the transistor (MOSFET) 10 shown in Fig. 1 is the structure shown in Fig. 2. (See column 2 line 61-67)

The structure of the device shown in Fig. 2 is used in such a condition that the n+ region 14 and P-type semiconductor material 26 (p-well) are connected to the ground (Vss). Therefore, it is quite clear that the n+ region 14 is a source region and the n+ region 12 is a drain region in the case of N-MOS FET of Fig. 2. Thus, the n-well 22 is formed under the drain region 12 in this case.

The structure of the device shown in Fig. 6 is another embodiment for the transistor (MOSFET) 10. (See column 5 line 24-35)

Therefore, the structure of the device shown in Fig. 6 is also used in such a condition that the n+ region 14 and p-type semiconductor material 26 (p-well) are connected to the ground (Vss). Of course, it is quite clear that the n+ region 14 is a source region and the n+ region 12 is a drain region in the case of N-MOS FET of Fig. 6. Thus, the n-well 22 is formed under the drain region 12 in the case of Fig. 6.

In this view, Duvvury teaches nothing about any device structure where the n-well is formed under the source region 14 for the case where the source 14 and p-well 26 (p-type

semiconductor substrate) are electrically connected to Vss (ground) level and the drain 12 is electrically connected to bias V.

Since applicant's admitted prior art and the references applied by the Examiner do not disclose applicant's recited claim limitations, the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. § 103. As such, the rejection must be withdrawn.

Conclusions:

It is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 12-13-04

By _____

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 672-5407
Facsimile: (202) 672-5399

David A. Blumenthal
Attorney for Applicant
Registration No. 26,257